

FORM PTO-892 (REV. 3-78)		U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE		SERIAL NO. <b>843454</b>	GROUP ART UNIT <b>114</b>	ATTACHMENT TO PAPER NUMBER <b>2</b>			
NOTICE OF REFERENCES CITED				APPLICANT(S) <b>BLACHARD</b>					
U.S. PATENT DOCUMENTS									
		DOCUMENT NO.	DATE	NAME	CLASS	SUB-CLASS	FILING DATE IF APPROPRIATE		
A		4582565	4-86	KAWAKATSU	29	580	8-8-84		
B		4509249	4-85	GOTO ET AL.	29	576W	9-23-83		
C		4374455	2-83	GOODMAN	29	580			
D		4546367	10-85	SCHUTTEN ET AL.	357	55	6-21-82		
E		4596999	6-86	GOBRECHT ET AL.	357	55	3-22-84		
F		4345265	8-80	BLACHARD	29	571			
G									
H									
I									
J									
K									
FOREIGN PATENT DOCUMENTS									
		DOCUMENT NO.	DATE	COUNTRY	NAME	CLASS	SUB-CLASS	PERTINENT SHTS. DWG.	PP. SPEC.
L		0065447	4-84	JAPAN	KAZUYA	29	576W		
M		0108325	6-84	JAPAN	TOSHIO	29	576W		
N									
O									
P									
Q									
OTHER REFERENCES (Including Author, Title, Date, Pertinent Pages, Etc.)									
R		UEDA, "A NEW VERTICAL POWER MOSFET STRUCTURE WITH EXTREMELY REDUCED ON-RESISTANCE," IEEE TRANS. ON ELECTRON DEVICES, VOL. ED-32, No. 1 Jan. 85 PP. 2-6.							
S		BALIGA, "THE INSULATED GATE TRANSISTOR, A NEW THREE-DIMENSIONAL TERMINAL MOS CONTROLLED DIPOLAR POWER DEVICE," IEEE TRANS. ON ELECT. DEV. VOL. ED-31, JUN. 84, PP. 821-828							
T									
U									
EXAMINER <b>T. Thomas.</b>			DATE <b>12-17-86.</b>						
*A copy of this reference is not being furnished with this office action. (See Manual of Patent Examining Procedure, section 707.05 (a).)									